

82430LX/82430NX PCIsset

- Supports the Pentium™ Processor at 60 and 66 MHz (82430LX)
- Supports the Pentium Processor at ICOMP™ Index 735/90 MHz and Pentium Processor at ICOMP Index 815/100 MHz
- Interfaces the Host and Standard Buses to the PCI Local Bus
 - Up to 132 MBytes/Sec Transfer Rate
 - Full Concurrency Between CPU Host Bus and PCI Bus Transactions
- Integrated Cache Controller Provided for Optional Second Level Cache
 - 256 KByte or 512 KByte Cache
 - Write-Back or Write-Through Policy (82430LX)
 - Write-Back Policy (82430NX)
 - Standard or Burst SRAM
- Integrated Tag RAM for Cost Savings on Second Level Cache
- Provides a 64-Bit Interface to DRAM Memory
 - From 2 MBytes to 512 MBytes of Main Memory
 - 70 ns and 60 ns DRAMs Supported
- Supports the Pipelined Address Mode of the Pentium Processor for Higher Performance
- Optional ISA or EISA Standard Bus Interface
 - Single Component ISA Controller
 - Two Component EISA Bus Interface
 - Minimal External Logic Required
- Supports Burst Read and Writes of Memory from the CPU and PCI Buses
- Five Integrated Write Posting and Read Prefetch Buffers Increase CPU and PCI Performance
- Host CPU Writes to PCI Converted to Zero Wait-State PCI Bursts with Optional TRDY# Connection
- Integrated Low Skew Host Bus Clock Driver for Cost and Board Space Savings
- PCIsset Operates Synchronous to the CPU and PCI Clocks
- Byte Parity Support for the Host and Main Memory Buses
 - Optional Parity on the Second Level Cache

The 82430LX/82430NX PCIssets provide the Host/PCI bridge, cache/main memory controller, and an I/O subsystem core (either PCI/EISA or PCI/ISA bridge) for the next generation of high-performance personal computers based on the Pentium processor. System designers can take advantage of the power of the PCI Local bus for the local I/O while maintaining access to the large base of EISA and ISA expansion cards, and corresponding software applications. Extensive buffering and buffer management within the bridges ensures maximum efficiency in all three bus environments (Host CPU, PCI, and EISA/ISA Buses).

The 82430LX PCIsset consists of the 82434LX PCI/Cache Memory Controller (PCMC) and the 82433LX Local Bus Accelerator (LBX) components, plus, either a PCI/ISA bridge or a PCI/EISA bridge. The PCMC and LBX provide the core cache and main memory architecture and serve as the Host/PCI bridge. For an ISA-based system, the 82430LX PCIsset includes the 82378IB System I/O (SIO) component as the PCI/ISA bridge. For an EISA-based system, the 82430LX PCIsset includes the 82375EB/SB PCI/EISA Bridge (PCEB) and the 82374EB/SB EISA System Component (ESC). The PCEB and ESC work in a tandem to form the complete PCI/EISA bridge. Both the ISA and EISA-based systems are shown on the following pages.

The 82430NX PCIsset consists of the 82434NX PCI/Cache Memory Controller (PCMC) and the 82433NX Local Bus Accelerator (LBX) components, plus, either a PCI/ISA bridge or a PCI/EISA bridge. For an ISA-based system, the 82430NX PCIsset includes the 82378ZB System I/O (SIO) component as the PCI/ISA bridge. For an EISA-based system, the 82430NX PCIsset includes the 82375EB/SB PCI/EISA Bridge (PCEB) and the 82374EB/SB EISA System Component (ESC).

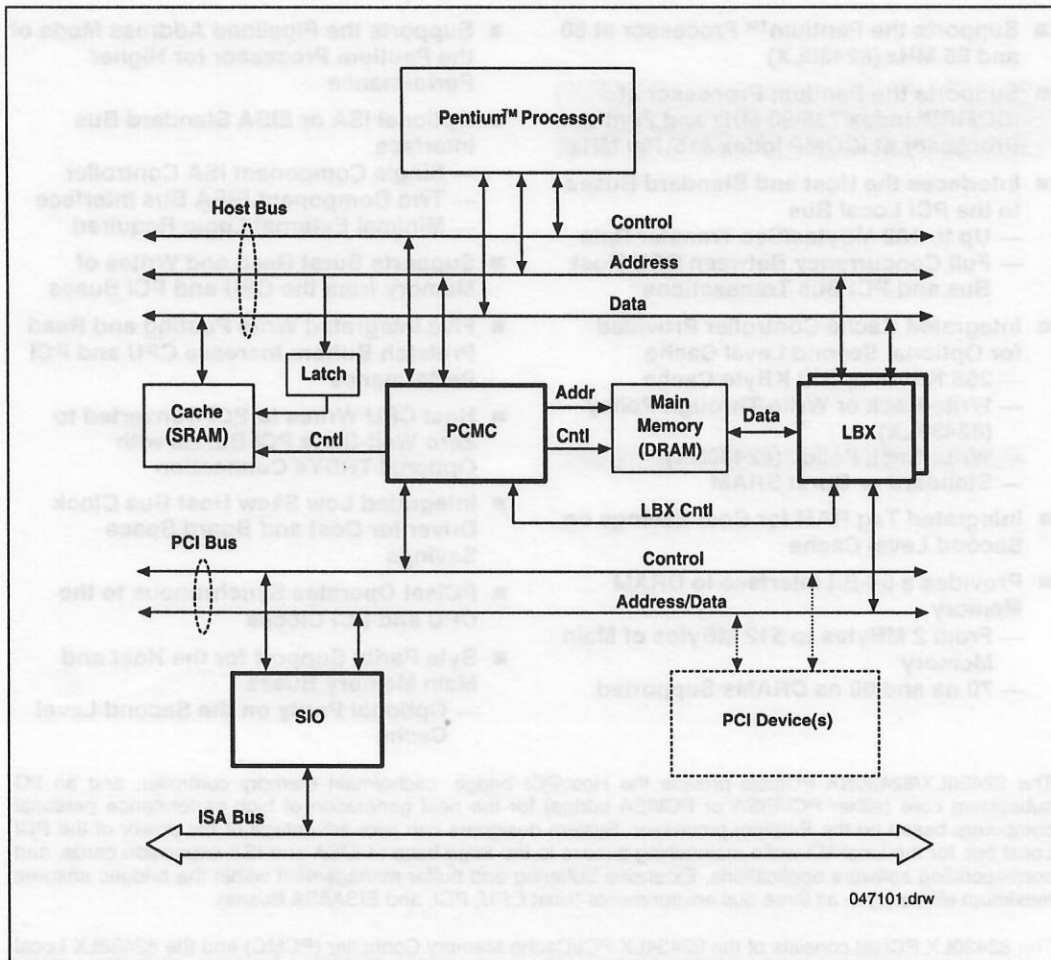
This document describes both the 82430LX and 82430NX. Unshaded areas describe the 82434LX. Shaded areas, like this one, describe 82430NX operations that differ from the 82434LX.

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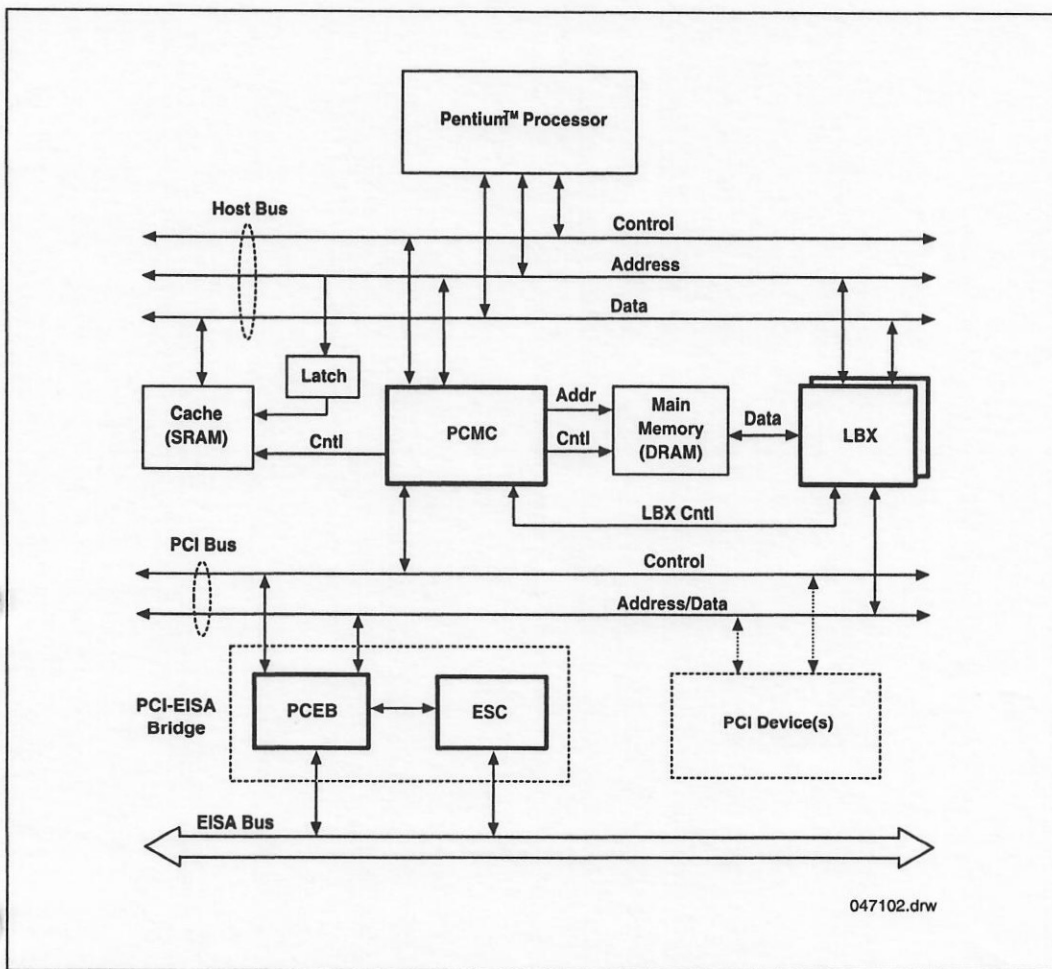
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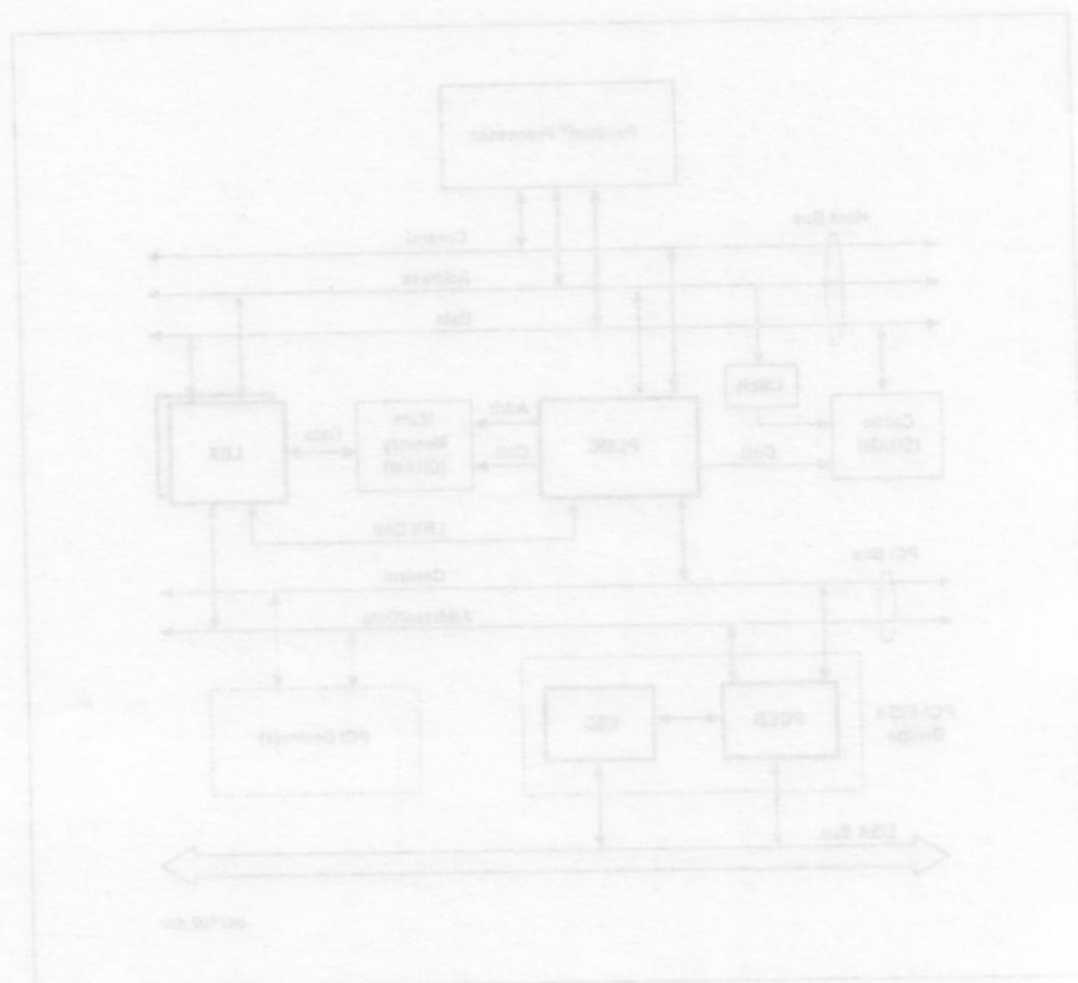
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82430LX or 82430NX PCIs et ISA Block Diagram



82430LX or 82430NX PCIsset EISA Block Diagram



82400X/82400X PCMCIA Block Diagram



82434LX/82434NX PCI, CACHE AND MEMORY CONTROLLER (PCMC)

- Supports the Pentium™ Processor at 60 and 66 MHz, and 50 MHz (82434NX only)
- Supports Pipelined Addressing Capability of the Pentium Processor
- The 82434NX Drives 3.3 V Signal Levels on the CPU and Cache Interfaces
- High Performance CPU/PCI/Memory Interfaces via Posted Write and Read Prefetch Buffers
- Fully Synchronous 33 MHz PCI Interface with Full Bus Master Capability
 - 82434LX Supports PCI Configuration Access Mechanisms #2
 - 82434NX Supports PCI Configuration Access Mechanisms #1 and #2
- Supports the Pentium Processor Primary Cache in Either Write-Through or Write-Back Mode
- Programmable Attribute Map of DOS and BIOS Regions for System Flexibility
- Integrated Low Skew Clock Driver for Distributing Host Clock
- Integrated Second Level Cache Controller
 - Integrated Cache Tag Ram
 - Write-Through and Write-Back Cache Modes for the 82434LX
 - Write-Back Only for the 82434NX
 - 82434NX Supports Low-Power Cache Standby
 - Direct Mapped Organization
 - Supports Standard and Burst SRAMs
 - 256 KByte and 512 KByte Sizes
 - Cache Hit Cycle of 3-1-1-1 on Reads and Writes Using Burst SRAMs (60 and 66 MHz)
 - 2-1-1-1 Reads and Writes at 50 MHz (82434NX Only)
 - Cache Hit Cycle of 3-2-2-2 on Reads and 4-2-2-2 on Writes Using Standard SRAMs, and
- 2-2-2-2 Reads/3-2-2-2 Writes at 50 MHz (82434NX Only)
- Integrated DRAM Controller
 - Supports 2 MByte to 192 MByte of Cacheable Main Memory for the 82434LX
 - Supports 2 MByte to 512 MByte of Cacheable Main Memory for the 82434NX
 - Supports DRAM Access Times of 70 and 60 ns
 - CPU Writes Posted to DRAM 4-1-1-1
 - Refresh Cycles Decoupled from ISA Refresh to Reduce the DRAM Access Latency
 - Six RAS# Lines (82434LX)
 - Eight RAS# Lines (82434NX)
 - Refresh by RAS#-Only, or CAS-Before-RAS#, in Single or Burst of Four
- Host/PCI Bridge
 - Translates CPU Cycles into PCI Bus Cycles
 - Translates Back-to-Back Sequential CPU Memory Writes into PCI Burst Cycles
 - Burst Mode Writes to PCI in Zero PCI Wait-States (i.e. Data Transfer Every Cycle)
 - Full Concurrency Between CPU-to-Main Memory and PCI-to-PCI Transactions
 - Full Concurrency Between CPU-to-Second Level Cache and PCI-to-Main Memory Transactions
 - Same Cache and Memory System Logic Design for ISA and EISA Systems
 - Cache Snoop Filter Ensures Data Consistency for PCI-to-Main Memory Transactions
- 208-Pin QFP Package

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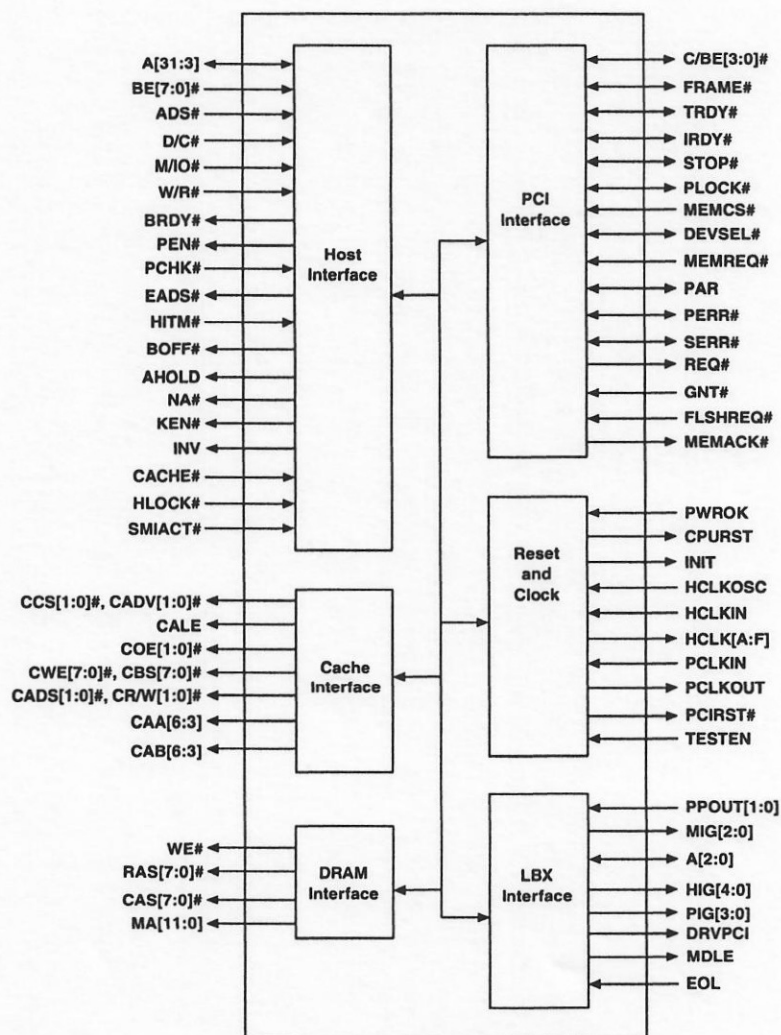
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The 82434LX/82434NX PCI, Cache, Memory Controllers (PCMC) integrate the cache and main memory DRAM control functions and provide bus control for transfers between the CPU, cache, main memory, and the PCI Local Bus. The cache controller supports write-back (or write-through for 82434LX) cache policy and cache sizes of 256 KBytes and 512 KBytes. The cache memory can be implemented with either standard or burst SRAMs. The PCMC cache controller integrates a high-performance Tag RAM to reduce system cost. For the 82434NX, up to sixteen single-sided SIMMs or eight double-sided SIMMs provide a maximum of 512 MBytes of main memory. For the 82434LX, up to 12 single-sided SIMMs or 6 double-sided SIMMs provide maximum of 192 MByte of main memory. The 82434NX PCMC is intended to be used with the 82433NX Local Bus Accelerator (LBX). The LBX provides the Host-to-PCI address path and data paths between the CPU/cache, main memory, and PCI. The LBX also contains posted write buffers and read-prefetch buffers. Together, these two components provide a full function data path to main memory and form a PCI bridge to the CPU/cache and DRAM subsystem.



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NOTE:

RAS[7:6]# and MA11 are only on the 82434NX. CCS[1:0] functionality is only on the 82434NX.

PCMC Simplified Block Diagram

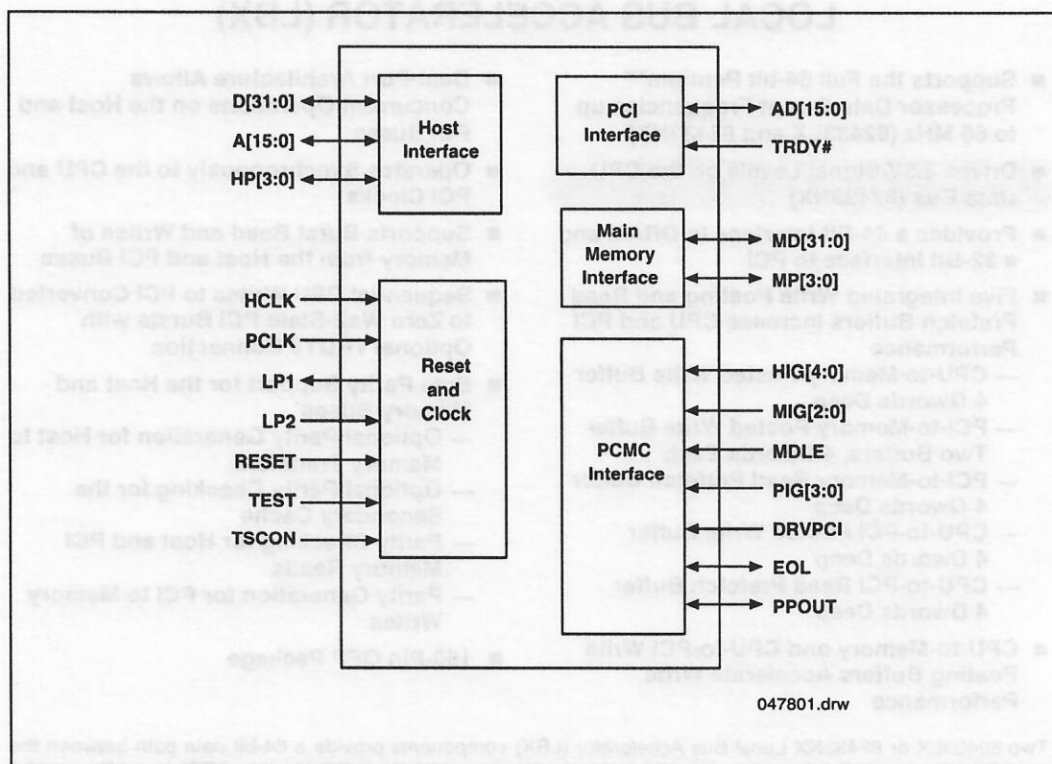
82433LX/82433NX

LOCAL BUS ACCELERATOR (LBX)

- Supports the Full 64-bit Pentium™ Processor Data Bus at Frequencies up to 66 MHz (82433LX and 82433NX)
- Drives 3.3V Signal Levels on the CPU Data Bus (82433NX)
- Provides a 64-Bit Interface to DRAM and a 32-Bit Interface to PCI
- Five Integrated Write Posting and Read Prefetch Buffers Increase CPU and PCI Performance
 - CPU-to-Memory Posted Write Buffer 4 Qwords Deep
 - PCI-to-Memory Posted Write Buffer Two Buffers, 4 Dwords Each
 - PCI-to-Memory Read Prefetch Buffer 4 Qwords Deep
 - CPU-to-PCI Posted Write Buffer 4 Dwords Deep
 - CPU-to-PCI Read Prefetch Buffer 4 Dwords Deep
- CPU-to-Memory and CPU-to-PCI Write Posting Buffers Accelerate Write Performance
- Dual-Port Architecture Allows Concurrent Operations on the Host and PCI Buses
- Operates Synchronously to the CPU and PCI Clocks
- Supports Burst Read and Writes of Memory from the Host and PCI Buses
- Sequential CPU Writes to PCI Converted to Zero Wait-State PCI Bursts with Optional TRDY# Connection
- Byte Parity Support for the Host and Memory Buses
 - Optional Parity Generation for Host to Memory Transfers
 - Optional Parity Checking for the Secondary Cache
 - Parity Checking for Host and PCI Memory Reads
 - Parity Generation for PCI to Memory Writes
- 160-Pin QFP Package

Two 82433LX or 82433NX Local Bus Accelerator (LBX) components provide a 64-bit data path between the host CPU/Cache and main memory, a 32-bit data path between the host CPU bus and PCI Local Bus, and a 32-bit data path between the PCI Local Bus and main memory. The dual-port architecture allows concurrent operations on the host and PCI Buses. The LBXs incorporate three write posting buffers and two read prefetch buffers to increase CPU and PCI performance. The LBX supports byte parity for the host and main memory buses. The 82433NX is intended to be used with the 82434NX PCI/Cache/Memory Controller (PCMC). The 82433LX is intended to be used with the 82434LX PCMC. During bus operations between the host, main memory and PCI, the PCMC commands the LBXs to perform functions such as latching address and data, merging data, and enabling output buffers. Together, these three components form a "Host Bridge" that provides a full function dual-port data path interface, linking the host CPU and PCI bus to main memory.

This document describes both the 82433LX and 82433NX. Shaded areas, like this one, describe the 82433NX operations that differ from the 82433LX.



LBX Simplified Block Diagram

82374EB/SB EISA SYSTEM COMPONENT (ESC)

- **Integrates EISA Compatible Bus Controller**
 - Translates Cycles Between EISA and ISA Bus
 - Supports EISA Burst and Standard Cycles
 - Supports ISA Zero Wait-State Cycles
 - Supports Byte Assembly/Disassembly for 8-, 16- and 32-Bit Transfers
 - Supports EISA Bus Frequency of up to 8.33 Mhz
- **Supports Eight EISA Slots**
 - Directly Drives Address, Data and Control Signals for Eight Slots
 - Decodes Address for Eight Slot Specific AENs
- **Provides Enhanced DMA Controller**
 - Provides Scatter-Gather Function
 - Supports Type A, Type B, Type C (Burst), and Compatible DMA Transfer
 - Provides Seven Independently Programmable Channels
 - Integrates Two 82C37A Compatible DMA Controllers
- **Integrates the Functionality of two 82C59 Interrupt Controllers and two 82C54 Timers**
 - Provides 14 Programmable Channels for Edge or Level Interrupts
 - Provides 4 PCI Interrupts Routable to any of 11 Interrupt Channels
 - Supports Timer Function for Refresh Request, System Timer, Speaker Tone, Fail Safe Timer, and CPU Speed Control
- **Advanced Programmable Interrupt Controller (APIC)**
 - Multiprocessor Interrupt Management
 - 33 MHz Operation
 - Dedicated Bus For Interrupt Messages
- **5 V CMOS Technology**
- **Provides High Performance Arbitration**
 - Supports Eight EISA Masters and PCEB
 - Supports ISA Masters, DMA Channels, and Refresh
 - Provides Programmable Arbitration Scheme for Fixed, Rotating, or Combination Priority
- **Integrates Support Logic for X-Bus Peripherals**
 - Generates Chip Selects/Encoded Chip Selects for Floppy and Keyboard Controller, IDE, Parallel/Serial Ports, and General Purpose Peripherals
 - Provides Interface for Real Time Clock
 - Generates Control Signals for X-Bus Data Transceiver
 - Integrates Port 92, Mouse Interrupt, and Coprocessor Error Reporting
- **Generates Non-Maskable Interrupts (NMI)**
 - PCI System Errors
 - PCI Parity Errors
 - EISA Bus Parity Errors
 - Fail Safe Timer
 - Bus Timeout
 - Via Software Control
- **Provides BIOS Interface**
 - Supports 512K Bytes of Flash or EPROM BIOS on the X Bus
 - Allows BIOS on PCI
 - Supports Integrated VGA BIOS
- **82374SB System Power Management (Intel SMM Support)**
 - Fast On/Off Support via SMI Generation—Hardware Events, Software Events, EXTSMI#, Fast Off Timer, System Events
 - Programmable CPU Clock Control
 - Enables Energy Efficient Desktop Systems
- **208-Pin QFP Package**

The 82374EB/SB EISA System Component (ESC) provides all the EISA system compatible functions. The ESC with the PCEB provide all the functions to implement an EISA-to-PCI bridge and EISA I/O subsystem.

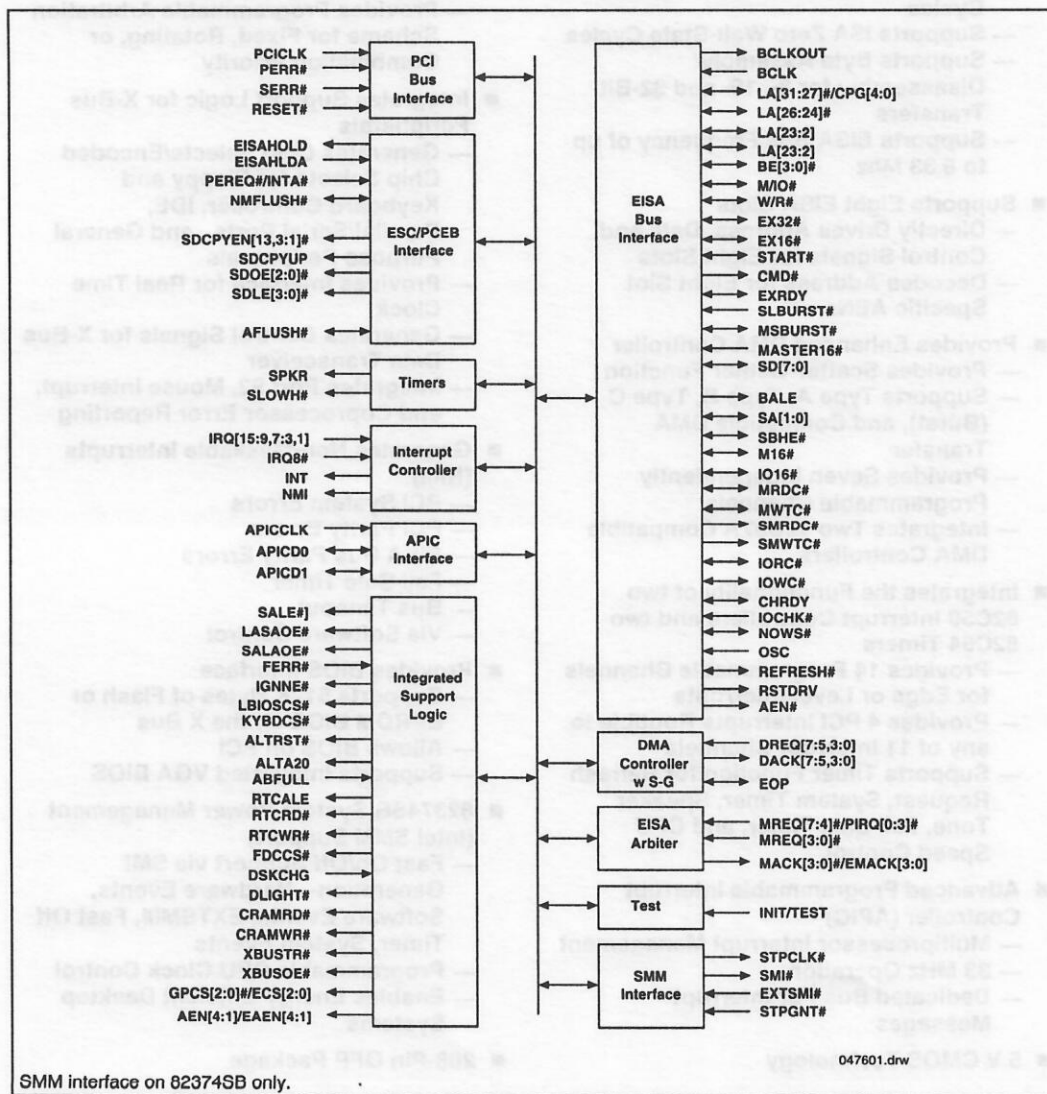
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The ESC integrates the common I/O functions found in today's EISA-based PC systems. The ESC incorporates the logic for an EISA (master and slave) interface, EISA bus controller, enhanced seven channel DMA controller with scatter-gather support, EISA arbitration, 14 channel interrupt controller, Advanced Programmable Interrupt Controller (APIC), five programmable timer/counters, and non-maskable-interrupt (NMI) control logic. The 82374SB ESC contains support for SMM power management. The ESC also integrates support logic to decode peripheral devices such as the Flash BIOS, real time clock, keyboard/mouse controller, floppy controller, two serial ports, one parallel port, and IDE hard disk drive.



ESC Simplified Block Diagram

82375EB/SB PCI-EISA BRIDGE (PCEB)

- Provides the Bridge Between the PCI Local Bus and EISA Bus
- 100% PCI and EISA Compatible
 - PCI and EISA Master/Slave Interface
 - Directly Drives 10 PCI Loads and 8 EISA Slots
 - Supports PCI from 25 to 33 MHz
- Data Buffers Improve Performance
 - Four 32-bit PCI-to-EISA Posted Write Buffers
 - Four 16-byte EISA-to-PCI Read/Write Line Buffers
 - EISA-to-PCI Read Prefetch
 - EISA-to-PCI and PCI-to-EISA Write Posting
- Data Buffer Management Ensures Data Coherency
 - Flush Posted Write Buffers
 - Flush or Invalidate Line Buffers
 - System-Wide Data Buffer Coherency Control
- Burst Transfers on both the PCI and EISA Buses
- 32-Bit Data Paths
- Integrated EISA Data Swap Buffers
- Arbitration for PCI Devices
 - Supports Six PCI Masters
 - Fixed, Rotating, or a Combination of the Two
 - Supports External PCI Arbiter and Arbiter Cascading
- PCI and EISA Address Decoding and Mapping
 - Positive Decode of Main Memory Areas (MEMCS# Generation)
 - Four Programmable PCI Memory Space Regions
 - Four Programmable PCI I/O Space Regions
- Programmable Main Memory Address Decoding
 - Main Memory Sizes up to 512 MBytes
 - Access Attributes for 15 Memory Segments in First 1 MByte of Main Memory
 - Programmable Main Memory Hole
- Integrated 16-bit BIOS Timer

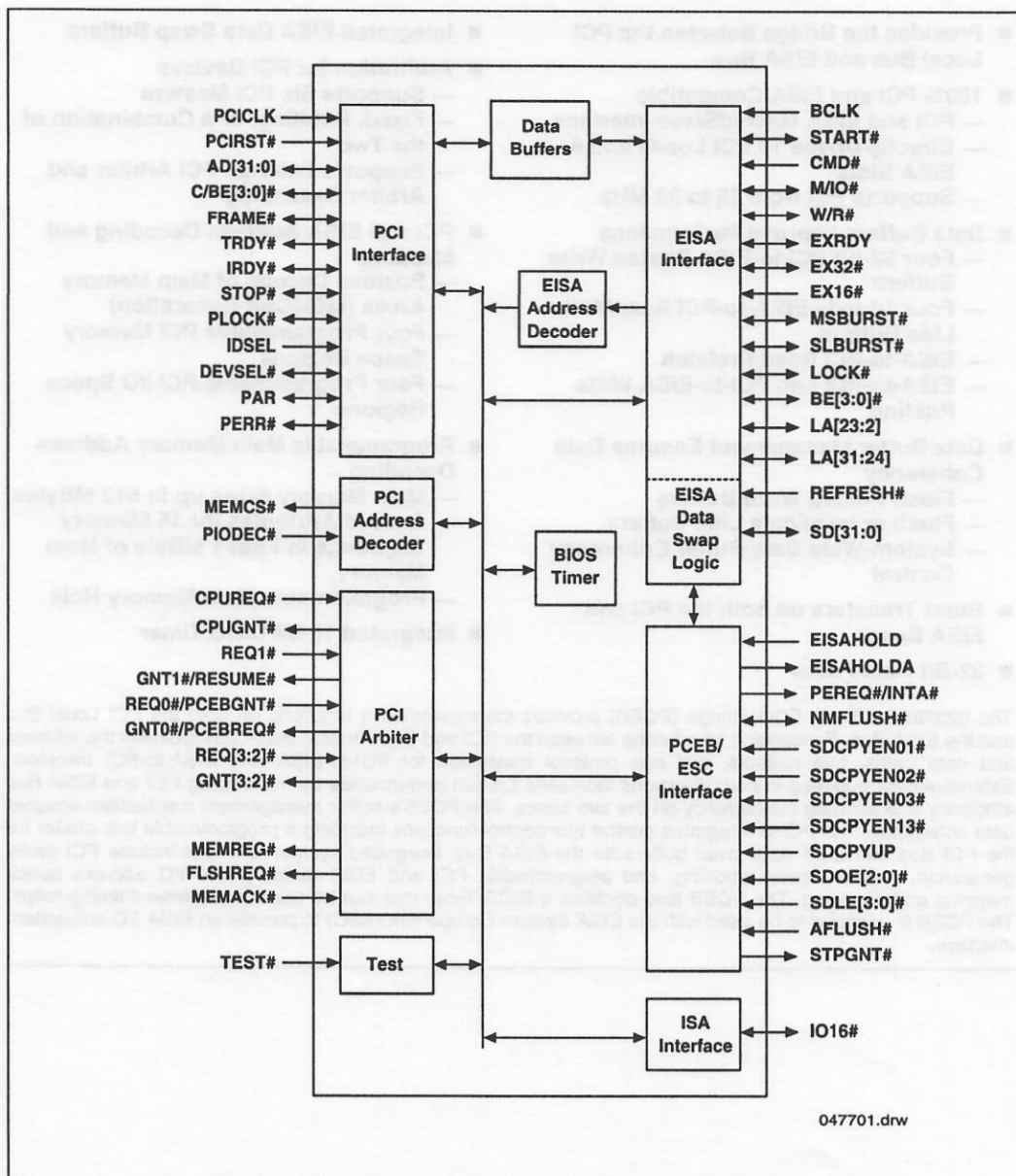
The 82375EB/SB PCI-EISA Bridge (PCEB) provides the master/slave functions on both the PCI Local Bus and the EISA Bus. Functioning as a bridge between the PCI and EISA buses, the PCEB provides the address and data paths, bus controls, and bus protocol translation for PCI-to-EISA and EISA-to-PCI transfers. Extensive data buffering in both directions increases system performance by maximizing PCI and EISA Bus efficiency and allowing concurrency on the two buses. The PCEB's buffer management mechanism ensures data coherency. The PCEB integrates central bus control functions including a programmable bus arbiter for the PCI Bus and EISA data swap buffers for the EISA Bus. Integrated system functions include PCI parity generation, system error reporting, and programmable PCI and EISA memory and I/O address space mapping and decoding. The PCEB also contains a BIOS Timer that can be used to implement timing loops. The PCEB is intended to be used with the EISA System Component (ESC) to provide an EISA I/O subsystem interface.

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PCEB Simplified Block Diagram



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